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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,251	HEPNER ET AL.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received June 23, 2006 for application number 10/671251 originally filed September 23, 2003. The Office hereby acknowledges that no new amended claims have been submitted. Therefore, the original, unamended claims originally submitted September 23, 2003 remain present for examination.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-4 and 11-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Chakravarthy et al. (U.S. Patent Publication No. 2004/0059956 A1) (hereinafter referred to as Chakravarthy).

As to claim 1, Chakravarthy discloses a microprocessor system comprising a CPU (120), a clock (PLL 208) providing a CLK signal to the CPU (paragraph, lines 5-7), a counter (within performance monitor 204) counting clock pulses to the CPU (paragraph 28, lines 1-4), and a monitor (performance monitor 204), wherein the clock (208) is adapted to provide a CLK signal to the counter (via 210) when a software task is running on the CPU (paragraph 28), said counter adapted to count the number of clock pulses since a RESET (signal PMCPUCLKUNHALTED# 222) (Chakravarthy discloses when a clock signal is asserted to CPU 120, the counter within the performance monitor 204 counts the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is asserted; paragraphs 27 and 28); the CPU is adapted (via PMON

circuit 200.2) to provide a RESET signal (PMCPUCLKUNHALTED# 222) to the counter for each CLK pulse when a software task is not running on the CPU (Chakravarthy discloses the counter within the performance monitor 204 does not count the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is de-asserted; paragraph 28); and the monitor is adapted to store the value in the counter immediately prior to the last RESET (Chakravarthy saving the counted clock pulses as "Time0" when a CPU_CLKS_UNHALTED event occurs; paragraph 36).

As to claim 2, Chakravarthy discloses the microprocessor system wherein the CPU is adapted (via PMON circuit 200.2) to block a RESET signal (PMCPUCLKUNHALTED#) to the counter when a software task is running on the CPU (Chakravarthy discloses when a clock signal is asserted to CPU 120, the counter within the performance monitor 204 counts the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is asserted; paragraphs 27 and 28).

As to claim 3, the microprocessor system wherein the CPU is adapted to continuously pass CLK signals (via 210) to the counter when a software task is running on the CPU (paragraphs 27 and 28).

As to claim 4, Chakravarthy discloses the microprocessor system wherein the CPU is adapted to pass a RESET signal (via PMON circuit 200.2) to the counter when is software task is not running on the CPU (paragraphs 26-28).

As to claim 11, Chakravarthy discloses a method of operating a microprocessor system, said system comprising a CPU (120), a counter (within performance monitor 204; paragraph 28, lines 1-4), a monitor (performance monitor 204), and a clock (PLL 208), and wherein the clock (208) provides a CLK signal train to the counter (via 210) while a software task is running on the

CPU (paragraph 28), the counter counting the number of clock pulses since a RESET (signal PMCPUCLKUNHALTED# 222) (Chakravarthy discloses when a clock signal is asserted to CPU 120, the counter within the performance monitor 204 counts the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is asserted ;paragraphs 27 and 28), the CPU providing (via PMON circuit 200.2) a RESET signal (PMCPUCLKUNHALTED# 222) to the counter for each CLK pulse when a software task is not running on the CPU (Chakravarthy discloses the counter within the performance monitor 204 does not count the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is de-asserted; paragraph 28), and the monitor storing the value of the counter prior to the last RESET (Chakravarthy saving the counted clock pulses as "Time0" when a CPU_CLKS_UNHALTED event occurs; paragraph 36).

As to claim 12, Chakravarthy discloses the method wherein the CPU blocks (via PMON circuit 200.2) the RESET signal (PMCPUCLKUNHALTED#) to the counter when a software task is running on the CPU (Chakravarthy discloses when a clock signal is asserted to CPU 120, the counter within the performance monitor 204 counts the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is asserted; paragraphs 27 and 28).

As to claim 13, Chakravarthy discloses the method wherein the CPU continuously passes CLK signals (via 210) to the counter when a software task is running on the CPU (paragraphs 27 and 28).

As to claim 14, Chakravarthy discloses the method wherein the CPU passes a RESET signal (via PMON circuit 200.2) to the counter when is software task is not running on the CPU

(paragraphs 26-28).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 5-10 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravarthy (as cited hereinabove) as applied to claims 1 and 11 above, and further in view of Terrell, II (U.S. Patent Publication No. 2004/0098631 A1) (hereinafter referred to as Terrell).

As to claim 5, Chakravarthy does not disclose the monitor of the microprocessor system is adapted to output a control signal responsive to monitor content.

Terrell teaches a system clock power management system wherein a clock controller (10 or 62) is adapted to output control signals (14) to processors within the system (20 and 24 or 50 and 52) to control the common clock to the processors dependent on processor usage and clock counts when processor is active (paragraphs 15 and 32).

It would have been obvious to one of ordinary skill of the art having the teachings of Chakravarthy and Terrell, at the time the invention was made to modify the performance monitor of Chakravarthy to include the ability to send control signals in response to monitored activity as taught by Terrell. One of ordinary skill in the art would be motivated to make this combination in order to give the ability of the performance monitor to output control signals in view of the teachings of Terrell, as doing so would give the added benefit of monitoring both common and shared processor clock usage between multiple processors instead of one (paragraphs 9 and 10).

As to claim 6, Terrell teaches the microprocessor system wherein the monitor is adapted to output a power control signal responsive to monitor content (Terrell discloses controlling the clock frequency to the processing elements thus controlling power; paragraph 15).

As to claim 7, the microprocessor system wherein the monitor is adapted to output a function control signal responsive to monitor content (Terrell teaches a method and system wherein the output control signals from the monitor circuit [clock controller] are in response to hardware interrupts received from the system; paragraph 46).

As to claim 8, the microprocessor system wherein the monitor is adapted to output a clock control signal responsive to monitor content (Terrell discloses controlling the clock frequency to the processing elements thus controlling power; paragraph 15).

As to claim 9, the microprocessor system wherein the monitor is adapted to output a control signal reducing power input to the CPU responsive to monitor content when the monitor content is below a threshold ("guard band" frequency) (paragraphs 13 and 53).

As to claim 10, the microprocessor system wherein the monitor is adapted to output a control signal reducing clock pulse input to the CPU responsive to count content when the monitor content is below a threshold (paragraph 53).

As to claim 15, Chakravarthy does not disclose the monitor of the method wherein the monitor outputs a control signal responsive to count content.

Terrell teaches a system clock power management system wherein a clock controller (10 or 62) is adapted to output control signals (14) to processors within the system (20 and 24 or 50 and 52) to control the common clock to the processors dependent on processor usage and clock counts when processor is active (paragraphs 15 and 32).

It would have been obvious to one of ordinary skill of the art having the teachings of Chakravarthy and Terrell, at the time the invention was made to modify the performance monitor of Chakravarthy to include the ability to send control signals in response to monitored activity as taught by Terrell. One of ordinary skill in the art would be motivated to make this combination in order to give the ability of the performance monitor to output control signals in view of the teachings of Terrell, as doing so would give the added benefit of monitoring both common and shared processor clock usage between multiple processors instead of one (paragraphs 9 and 10).

As to claim 16, the method wherein the monitor outputs a power control signal responsive to monitor content (Terrell discloses controlling the clock frequency to the processing elements thus controlling power; paragraph 15).

As to claim 17, the method wherein the monitor outputs a function control signal responsive to monitor content (Terrell teaches a method and system wherein the output control signals from the monitor circuit [clock controller] are in response to hardware interrupts received from the system; paragraph 46).

As to claim 18, the method wherein the monitor outputs a clock control signal responsive to monitor content (Terrell discloses controlling the clock frequency to the processing elements thus controlling power; paragraph 15).

As to claim 19, the method wherein the monitor outputs a control signal reducing power input to the CPU responsive to monitor content when the monitor content is below a threshold ("guard band" frequency) (paragraphs 13 and 53).

As to claim 20, the method wherein the monitor outputs a control signal reducing clock speed of the CPU responsive to monitor content when the monitor content is below a threshold (paragraph 53).

Response to Arguments

Applicant's arguments filed June 23, 2006 to claims 1-20 have been fully considered but they are not persuasive.

As to the arguments directed to independent claims 1 and 11 (for claims 1-4 and 11-14), they have been fully considered but are not persuasive. The Applicant argues that Chakravarthy (as cited hereinabove) does not recite the element "the CPU is adapted to provide a RESET signal to the counter from each CLK pulse when a software task is not running." The Examiner respectfully disagrees with the Applicant's arguments for the following reasons:

The Applicant pointed out that the reset signal (PMCPUCLKUNHALTED# signal) of Chakravarthy was not the same as the RESET signal of the present invention. However, Chakravarthy discloses that the PMCPUCLKUNHALTED# is a signal created by the clock control unit (200.1) from signals (HLT 216 and BREAK 218) sent from the CPU (120) (paragraph 26). Therefore, PMCPUCLKUNHALTED# is provided, indirectly, by the CPU. Chakravarthy further discloses the performance monitor (204) which is inclusive of a counter (paragraph 28, lines 1-4) that measures a length of time (elapsed time) by counting the number of clock signals (ticks) and using two saved count values (Time0 and Time1) to determine the length of time (paragraphs 28 and 38). Chakravarthy further discloses that ***when the CPU is not performing work (not executing application code)*** that it measures a length of time (counts the

number of clock signals--*ticks*) that the RESET signal (PMCPUCLKUNHALTED#) is asserted (paragraph 28). Therefore, the Examiner respectfully asserts that Chakravarthy ***does anticipate*** "the CPU is adapted to provide a RESET signal to the counter from each CLK pulse when a software task is not running."

The Applicant further argued, in re claims 1 and 11, that the PMCPUCLKUNHALTED# signal does not reset the counter to zero. First, the Examiner would like to point out that nowhere in the claims (1 or 11) does it recite ***the counter being reset*** or that ***the counter is being reset to zero***. The claims only recite that "the CPU is adapted to provide a RESET signal to the counter" but does not recite that ***the counter is reset*** or that ***the counter is reset to zero***. Chakravarthy discloses the performance monitor (204) counts the number of clock signals (measures a length of time as argued hereinabove) when the RESET signal (PMCPUCLKUNHALTED#) is asserted when the CPU is not executing application codes (as argued hereinabove). Furthermore, Chakravarthy discloses that the performance monitor (counter) is reset (step 604) between measuring of elapsed time periods (using clock "ticks"--counts) when the RESET signal (PMCPUCLKUNHALTED#) is asserted (paragraphs 28 and 38). Furthermore, the Examiner respectfully disagrees with the Applicant's argument that the reference "requires an additional system timer to properly function" (Applicant's Response from June 23, 2006; page 3, lines 23-26). In re figures 5 and 6 of Chakravarthy are flowcharts used to show the inventive steps of the reference. Nowhere in Chakravarthy does it recite or necessitate "additional system timers" to accomplish the inventive tasks. However, Chakravarthy does disclose variables (Time0 and Time1) used to store the counter values for calculating the elapsed time which necessitates the counting of clock pulses (ticks) as argued above. In addition, the Applicant further argues that

the present invention "directly utilizes a count value to continuously enhance the efficiency of the system by adjusting control signals based on the count value" (Applicant's Response from June 23, 2006; page 3, lines 28-30). However, nowhere is such an element claimed in claims 1 or 11.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "directly utilizes a count value to continuously enhance the efficiency of the system by adjusting control signals based on the count value" and "the counter being reset" or that "the counter is being reset to zero") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Therefore, Chakravarthy teaches each and every element recited in claims 1 and 11. Hence, the Office Action submitted March 23, 2006 did establish a proper *prima facie* case of anticipation.

Given the dependence of claims 2-10 and 12-20 on claims 1 and 11, they remain rejected as noted above and overcome the arguments of the Applicant.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
August 31, 2006

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